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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	08/530,661
Filing Date	September 20, 1995
First Named Inventor	Keeth et al.
Group Art Unit	2814
Examiner Name	D. Wille
Attorney Docket Number	2269-5990US

ENCLOSURES *(check all that apply)*

- ☒ Postcard receipt acknowledgment (attached to the front of this transmittal)
- ☐ Duplicate copy of this transmittal sheet in the event that additional filing fees are required under 37 C.F.R. § 1.16
- ☐ Preliminary Amendment
- ☐ Response to Restriction Requirement/Election of Species Requirement dated
- ☐ Amendment in response to office action dated
- ☐ Amendment under 37 C.F.R. § 1.116 in response to final office action dated
- ☐ Additional claims fee - Check No. in the amount of $
- ☐ Letter to Chief Draftsman and copy of FIGS. with changes made in red
- ☐ Transmittal of Formal Drawings
- ☐ Formal Drawings (sheets)
- ☐ Information Disclosure Statement, PTO/SB/08A; ☐ copy of cited references
- ☐ Supplemental Information Disclosure Statement; PTO/SB/08A; copy of cited references and Check No. in the amount of $180.00
- ☐ Associate Power of Attorney
- ☐ Petition for Extension of Time and Check No. in the amount of $
- ☐ Petition
- ☐ Fee Transmittal Form
- ☐ Certified Copy of Priority Document(s)
- ☐ Assignment Papers *(for an Application)*
- ☐ Terminal Disclaimer
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- ☒ Other Enclosure(s) *(please identify below)*:

  REPLY BRIEF (IN TRIPLICATE) in response to Examiner's Answer dated August 11, 2004

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Kevin K. Johanson	Registration No. 38,506
Signature		
Date	September 9, 2004	

CERTIFICATE OF MAILING

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Date of Deposit: September 9, 2004

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Keeth et all.

Serial No.: 08/530,661

Filed: September 20, 1995

For: SEMICONDUCTOR MEMORY CIRCUITRY

Confirmation No.: 5492

Examiner: D. Wille

Group Art Unit: 2814

Attorney Docket No.: 2269-5990US
(95-0424.00/US)

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REPLY BRIEF

Commissioner of Patents and Trademarks
Alexandria, VA 22313-1450

Attention: Board of Patent Appeals and Interferences

Sirs:

Pursuant to 37 C.F.R. § 1.193(b)(1), this Reply Brief is filed in triplicate in response to the Examiner's Answer mailed on August 11, 2004. This Reply Brief is submitted within two months of the mailing date of the Examiner's Answer pursuant to 37 C.F.R. § 1.193(b)(1).

APPELLANTS' REPLY TO EXAMINER'S RESPONSE TO ARGUMENT

As set forth in detail in Appellants' Appeal Brief, Appellant maintains that the Examiner has failed to establish a *prima facie* case of obviousness because the cited references to not teach or suggest all the claim limitations and the Examiner has not provided a motivation to combine the cited references to produce the claimed invention. The motivation to combine proposed by the Examiner is improper and, therefore, does not establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a).

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,838,038 to Takashima et al. in View of U.S. Patent No. 5,610,418 to Eimori; U.S. Patent No. 5,654,577 to Nakamura et al.; and U.S. Patent No. 5,287,000 to Takahashi et al.

Claims 6 through 10, 18, 19, 22, 23, 25 and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takashima et al. (U.S. Patent No. 5,838,038) in view of Eimori (U.S. Patent No. 5,610,418); Nakamura et al. (U.S. Patent No. 5,654,577); and Takahashi et al. (U.S. Patent No. 5,287,000). The teachings of the cited references are summarized in Appellant's Appeal Brief on pages 6 through 7.

Appellant's respectfully submits that the 35 U.S.C. § 103(a) obviousness rejections of claims 6 through 10, 18, 19, 22, 23, 25 and 26 are improper because, at the very least, the cited prior art does not teach or suggest all the claim limitations in sufficient detail that would enable a

combination of the references to result in any operable combination to establish a prima facie case of obviousness regarding the claimed invention.

The Examiner's proposed combination of "a DRAM of cell size of $2Fx3F=6F^2$" of Takashima ('038) (col. 25, lines 17-18) with a design rule of adequate reduction, such as a 0.25 micron design rule from Eimori is improper. Specifically, while Takashima discloses that "a DRAM of cell size of $2Fx3F=6F^2$ in which random access can be made and noise is small and which has trench capacitor type memory cells can be realized" (col. 25, lines 17-20), there is no disclosure of any specific design rule for allowing any specific memory cell densities. Therefore, the Examiner has derived a specific design rule, namely 0.25 microns, as a design rule that would result in densities in accordance with those of the claimed invention. However, neither Eimori nor Takashima, either individually or in any proper combination, disclose how to make a $6F^2$ memory cell using the design rule of 0.25 microns since the problems and solutions associated with shrinking Takashima's $6F^2$ memory cell are not disclosed.

Appellant respectfully disagrees that substitutions of the various components of the cited refernces is taught or suggested. The substitutions that the Examiner proposes as being obvious is a considerable oversimplification of semiconductor process technology. The Examiner errs in assuming that processes may simply be substituted at will into various designs. Appellant reiterates that Takashima does not even hint at disclosing the technology to implement the dimensions as proposed nor is there any hint at how such a combination could be integrated. In order to implement an enabling embodiment of the present technology, significant attention must be paid to lines and pitches and spaces which affect essentially all aspects of the design,

including active areas, spaces, pitches polysilicon and metal layers. It doesn't necessarily follow that one can apply an $8F^2$ technology to a $6F^2$ design. (Appellant notes that currently, only the assignee of record has memory devices in production that utilize $6F^2$ design as the implementation of such is not elementary nor is the substitution of such design specifications.)

Appellant respectfully asserts that 0.25 microns as a minimum feature size is NOT the only factor for calculating the array size. The array size is based upon pitch as well. Therefore, while features may approach 0.25 microns, the companion features are on the order of 0.35 microns or larger. Therefore the array size is actually calculated based upon row and column pitches which dictate the cell size, and not the minimum feature size. Specifically, in reference to Eimori, and to a memory cell as illustrated in FIG. 6 of Eimori, even though the illustrated design may be considered "0.25 micron" because the smallest feature size is 0.25 micron, the dimensions illustrate that the pitch is actually 0.35 micron and what is actually printed in the drawings of Eimori is 0.25 and 0.35 microns. Therefore, the array size is much larger and is not the $6mm^2$ as previously alleged by the Examiner.

Regarding the Takashima ('038) patent, Takashima does not discuss specific dimensions of semiconductor devices. Application of a process such as Eimori to Takashima would require significant process changes or at least significant experimentation, if at all possible.

As disclosed in Appellant's specification, shrinkage of the memory cell, whether $8F^2$ or $6F^2$, to reach a 0.6 micron memory cell pitch involves a number of significant problems. (Appellant's specification p. 2, line 19). As one example, as the minimum pitch falls below 1.0 micron, conventional "LOCal Oxidation of exposed Silicon" (LOCOS) techniques fail due to

excessive encroachment of the oxide beneath the masking stack. (Appellant's specification p. 7, lines 13-16). Furthermore, the memory cell storage node capacitance tends to decrease with the decrease in cell size, yet a minimum storage capacity for stored charge is required to maintain reliable operation. (Appellant's specification p. 8, lines 5-7). As yet another example of scaling issues, adequate spacing is required between adjacent devices, such as between a bit line contact and construction of a capacitor. (Appellant's specification p. 20, lines 3-6). Furthermore, field oxide regions, such as field oxide that is used to provide electrical isolation between certain adjacent banks of memory cells within an array, need to be eliminated to reduce size. (Appellant's specification p. 26, lines 7-11).

Additionally, bit line circuitry and bit line spacing affects the feasibility of shrinking an individual memory cell design within an array to a $6F^2$ size. (Appellant's specification p. 27, line 23 to p. 28, line 1). Furthermore, the space consumed by the digit lines D and D* and their associated circuitry become one of the limiting factors for conversion to a $6F^2$ size. (Appellant's specification p. 28, lines 15-17). All of the aforementioned design considerations would need to be addressed in order for the memory cell as disclosed by Takashima to be shrunk to a 0.6um memory cell resulting in the densities as claimed by Appellant in independent claim 6. As a further example, the memory cell of Takashima as illustrated in Figure 28, includes LOCOS isolation, illustrated as oxide 133 under the word lines and between adjacent memory cells, with spacing also illustrated between bit line contacts and storage nodes. A simple reduction in the photolithographic feature size would result in the problems that are identified and addressed only by Appellant's invention as claimed.

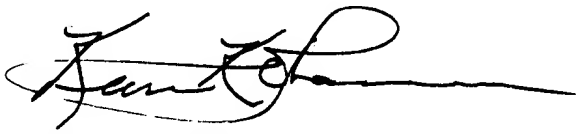
CONCLUSION

Claims 6 through 10, 18, 19, 22, 23, 25, and 26 are nonobvious under 35 U.S.C. § 103(a) and, thus, allowable over the asserted combination of teachings from Takashima et al. (U.S. Patent No. 5,838,038); Eimori (U.S. Patent No. 5,610,418); Nakamura et al. (U.S. Patent No. 5,654,577); and Takahashi et al. (U.S. Patent No. 5,287,000).

Reversal of the 35 U.S.C. § 103(a) rejections of claims 6 through 10, 18, 19, 22, 23, 25, and 26 is respectfully requested, and allowance of claims 6 through 10, 18, 19, 22, 23, 25, and 26 is further requested.

Pursuant to 37 C.F.R. § 1.193(b)(1), Appellant respectfully requests acknowledgement of receipt and entry of this Reply Brief.

Respectfully submitted,



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Date: September 9, 2004

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